

	No. 3033A	LC66512B, 66516B 12K-Byte/16K-Byte ROM-Contained Single-Chip 4-Bit Microcomputer for Control-Oriented Applications

General Description

The LC66512B, 66516B are 64-pin package type CMOS 4-bit single-chip microcomputers. They contain a ROM, a RAM, I/O ports, a dual 8-bit serial interface, a 4-channel comparator input, a dual 3-level input port, a 12-bit timer, an 8-bit timer, and provide 11 interrupt sources with 8 vector addresses.

Features

- (1) On-chip 12K-byte/16K-byte ROM, 512x4-bit RAM
- (2) Instruction set with 128 instructions extended from that of the LC6500 series
- (3) I/O ports ----- 58 pins
- (4) 8-bit serial interface ----- 2 lines (16-bit cascade connection available)
- (5) Minimum instruction cycle time ----- 0.92 μ s (4.3MHz external clock input mode)
- (6) Powerful timer function and prescaler
 12-bit timer-used interval timer, event counter, pulse width measurement, burst pulse output
 8-bit timer-used interval timer, event counter, PWM output, burst pulse output
 12-bit prescaler-used time base function
- (7) Powerful 11-source 8-vector interrupt function
 External interrupt: 6 sources, 3 vector addresses
 Internal interrupt: 5 sources, 5 vector addresses (timer: 2 sources, serial I/O: 2 sources, prescaler)
- (8) Flexible I/O function
 Comparator input, 3-level input, 20mA drive output, 15V breakdown voltage, pull-up/open drain selectable by option
- (9) Runaway detection function (option)
- (10) 8-bit input/output function
- (11) HALT/HOLD mode-used power-down function
- (12) Package: DIP64S, QFP64A (QIP64A)
- (13) Evaluation LSI: LC66599 (evaluation chip) + EVA850/800-TB665XX, LC66PG5XX (piggyback)
 LC66P516 microcontroller with built-in OT-PROM
 LC66E516 microcontroller with built-in EPROM

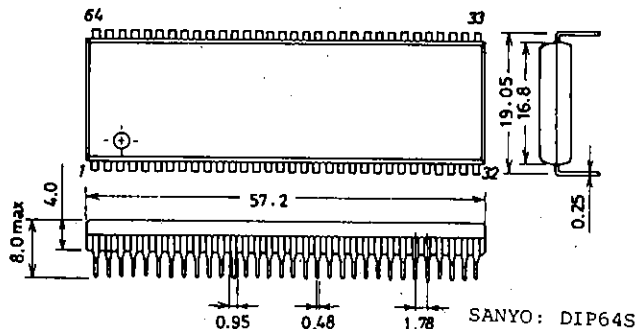
Note: The LC66512B, 66516B are different from the LC66512A, 66516A in the external constants for RC

Series Lineup

Type No.	Pins	ROM capacity	RAM capacity	Package	Remark
LC66304A/306A/308A	42,48	4K/6K/8KB	512W	DIP42S, QFP48E	Available
LC66354A/356A/358A	42,48	4K/6K/8KB	512W	DIP42S, QFP48E	Available
LC66354S/356S/358S	44	4K/6K/8KB	512W	QFP44M	Under development
LC66E308	42,48	EPROM 8KB	512W	DIC42S, QFC48 with window	Available
LC66P308	42,48	OTPROM 8KB	512W	DIP42S, QFP48E	Available
LC66404A/406A/408A	42,48	4K/6K/8KB	512W	DIP42S, QFP48E	Available
LC66E408	42,48	EPROM 8KB	512W	DIC42S, QFC48 with window	Available
LC66P408	42,48	OTPROM 8KB	512W	DIP42S, QFP48E	Available
LC66506B/508B/512B/516B	64	6K/8K/12K/16KB	512W	DIP64S, QFP64A	Available
LC66556A/558A/562A/566A	64	6K/8K/12K/16KB	512W	DIP64S, QFP64E	Available
LC66354B/356B/358B	42,48	4K/6K/8KB	512W	DIP42S, QFP48E	Available
LC66556B/558B	64	6K/8K	512W	DIP64S, QFP64E	Under development
LC66562B/566B	64	12K/16KB	512W	DIP64S, QFP64E	Available
LC66E516	64	EPROM 16KB	512W	DIC64S, QFC64 with window	Available
LC66P516	64	OTPROM 16KB	512W	DIP64S, QFP64E	Available

Package Dimensions 3071

(unit: mm)



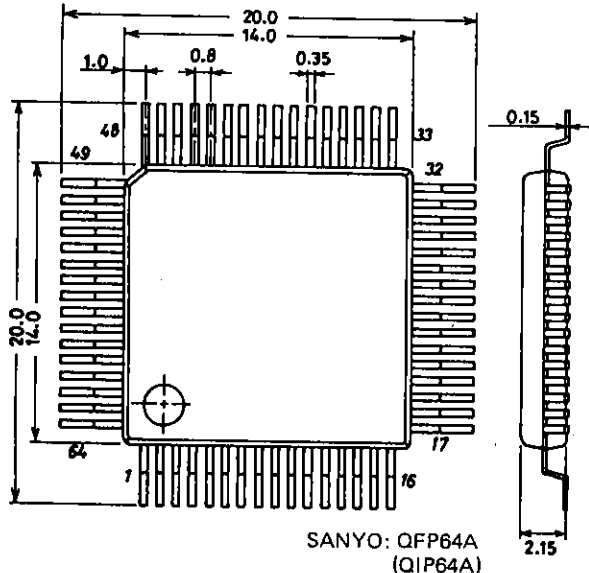
Pin Assignment

DIP64S

SI0/P20	1	64	VDD
S00/P21	2	63	P13
SCK0/P22	3	62	P12
INT0/P23	4	61	P11
INT1/P30	5	60	P10
POUT0/P31	6	59	P03
POUT1/P32	7	58	P02
HOLD/P33	8	57	P01
P40	9	56	P00
P41	10	55	PE1/TRB
P42	11	54	PE0/TRA
P43	12	53	PD3/CMP3
P50	13	52	PD2/CMP2
P51	14	51	PD1/CMP1
P52	15	50	PD0/CMP0
P53	16	49	PC3/VREF1
SI1/P60	17	48	PC2/VREF0
S01/P61	18	47	PC1
SCK1/P62	19	46	PC0
PIN1/P63	20	45	PB3
P70	21	44	PB2
P71	22	43	PB1
P72	23	42	PB0
P73	24	41	PA3
P80	25	40	PA2
P81	26	39	PA1
P82	27	38	PA0
P83	28	37	P93/INT5
INT2 P90	29	36	P92/INT4
TEST	30	35	P91 INT3
VSS	31	34	RES
OSC1	32	33	OSC2

Package Dimensions 3057

(unit: mm)



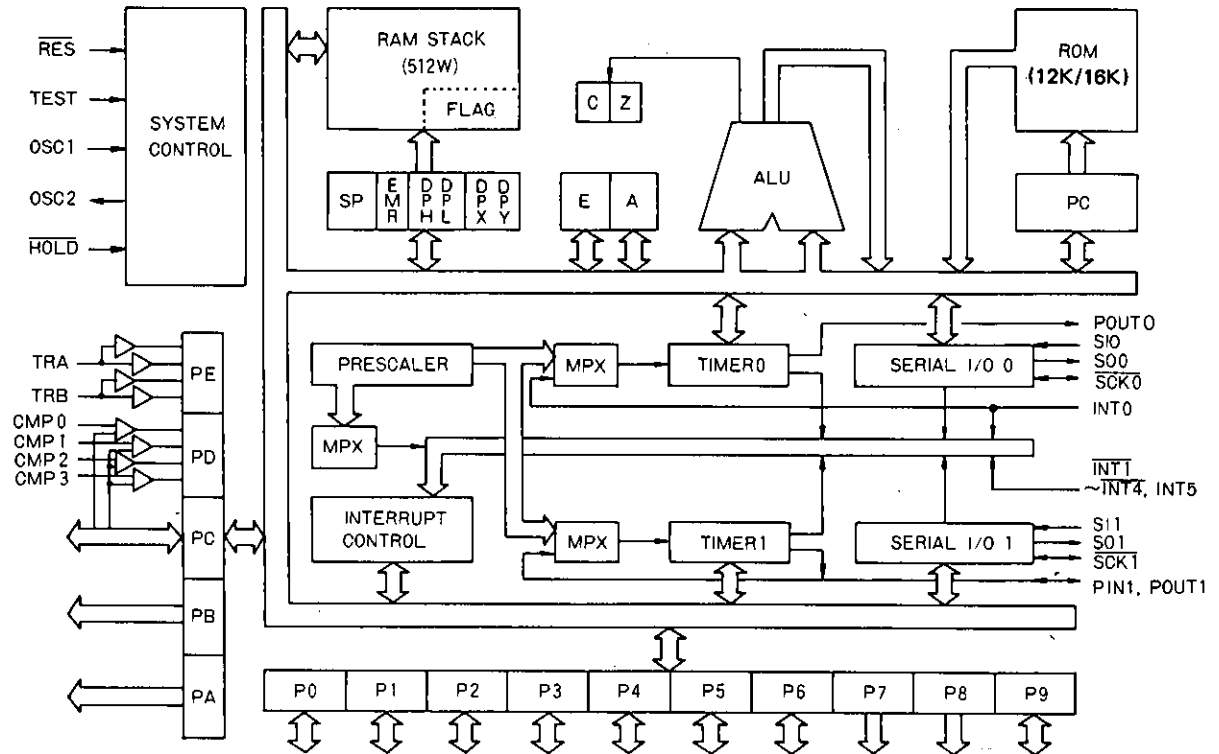
Pin Assignment

QFP64 (QIP64)

SI0/P20	1	64	VDD
S00/P21	2	63	P13
SCK0/P22	3	62	P12
INT0/P23	4	61	P11
INT1/P30	5	60	P10
POUT0/P31	6	59	P03
POUT1/P32	7	58	P02
HOLD/P33	8	57	P01
P40	9	56	P00
P41	10	55	PE1/TRB
P42	11	54	PE0/TRA
P43	12	53	PD3/CMP
P50	13	52	PD2/CMP
P51	14	51	PD1/CMP
P52	15	50	PD0/CMP
P53	16	49	PC3/VRE
SI1/P60	17	48	PC2/VRE
S01/P61	18	47	PC1
SCK1/P62	19	46	PC0
PIN1/P63	20	45	PB3
P70	21	44	PB2
P71	22	43	PB1
P72	23	42	PB0
P73	24	41	PA3
P80	25	40	PA2
P81	26	39	PA1
P82	27	38	PA0
P83	28	37	P93/INT5
INT2 P90	29	36	P92/INT4
TEST	30	35	P91 INT3
VSS	31	34	RES
OSC1	32	33	OSC2

Note) Reflow soldering is recommended for QFP (QIP) packages.
Please consult your local representative for information on solder-bath immersion of the device.

System Block Diagram



Pin Description

Pin Name	I/O	Functions	Output Driver Type	Option	During Reset
P00 P01 P02 P03	I/O	Input/output common port P00 to P03 • 4-bit and single-bit input/output • P00 to P03: Provided with HALT mode control function	• Pch: Pu MOS type • Nch: Small sink current type	• With Pu MOS or Nch OD output • Output level during reset	H or L (option)
P10 P11 P12 P13	I/O	Input/output common port P10 to P13 • 4-bit and single-bit input/output	• Pch: Pu MOS type • Nch: Small sink current type	• With Pu MOS or Nch OD output • Output level during reset	H or L (option)
P20/SIO P21/SO0 P22/SCK0 P23/INT0	I/O	Input/output common port P20 to P23 • 4-bit and single-bit input/output • P20: Common with serial input SIO • P21: Common with serial output SO0 • P22: Common with serial clock SCK0 • P23: Common with INT0 interrupt and timer 0-used event count, pulse width measurement input	• Pch: CMOS type • Nch: Small sink current type • +15V breakdown voltage at Nch OD configuration	• CMOS or Nch OD output	H
P30/INT1 P31/POUT0 P32/POUT1	I/O	Input/output common port P30 to P32 • 3-bit and single-bit input/output • P30: Common with INT1 interrupt request • P31: Common with burst pulse output from timer 0 • P32: Common with burst pulse output, PWM output from timer 1	• Pch: CMOS type • Nch: Small sink current type • +15 breakdown voltage at Nch OD configuration	• CMOS or Nch OD output	H
P33/HOLD	I	HOLD mode control input • The HOLD mode is entered by executing the HOLD instruction at $\overline{\text{HOLD}}=\text{L}$. • The CPU is restarted by setting the HOLD to H level at the HOLD mode. • Usable as input port P33 with P30 to P32 • Even if the $\overline{\text{RES}}$ is brought to L level when the P33/HOLD is at L level, the CPU is not reset. So this pin must be H level when V_{DD} has risen to a point where the CPU can operate properly.			

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Pin Name	I/O	Functions	Output Driver Type	Option	During Reset
P40 P41 P42 P43	I/O	Input/output port P40 to P43 • 4-bit and single-bit input/output • 8-bit input/output with P50 to P53 • 8-bit output of ROM data with P50 to P53	• Pch: Pu MOS type • Nch: Small sink current type	• With Pu MOS or Nch OD output	H
P50 P51 P52 P53	I/O	Input/output port P50 to P53 • 4-bit and single-bit input/output • 8-bit input/output with P40 to P43 • 8-bit output of ROM data with P40 to P43	• Pch: Pu MOS type • Nch: Small sink current type	• With Pu MOS or Nch OD output	H
P60/SI1 P61/SO1 P62/SCK1 P63/PIN1	I/O	Input/output common port P60 to P63 • 4-bit and single-bit input/output • P60: Common with serial input SI1 • P61: Common with serial output SO1 • P62: Common with serial clock SCK1 • P63: Common with event counter input of timer 1	• Pch: CMOS type • Nch: Small sink current type • +15V breakdown voltage at Nch OD configuration	• CMOS or Nch OD output	H
P70 P71 P72 P73	O	Output-only port P70 to P73 • 4-bit and single-bit output • When an input instruction is executed, the contents of the output latch are input.	• Pch: Pu MOS type • Nch: Medium sink current type • +15V breakdown voltage at Nch OD configuration	• With Pu MOS or Nch OD output	H
P80 P81 P82 P83	O	Output-only port P80 to P83 • 4-bit and single-bit output • When an input instruction is executed, the contents of the output latch are input. • Pch OD output option available	• Pch: CMOS type • Nch: Small sink current type	• CMOS or Pch OD output • Output level during reset	H or L (option)
P90/INT2 P91/INT3 P92/INT4 P93/INT5	I/O	Input/output common port P90 to P93 • 4-bit and single-bit input/output • P90: Common with INT2 interrupt request • P91: Common with INT3 interrupt request • P92: Common with INT4 interrupt request • P93: Common with INT5 interrupt request	• Pch: CMOS type • Nch: Small sink current type	• CMOS or Nch OD output	H

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Pin Name	I/O	Functions	Output Driver Type	Option	During Reset
PA0 PA1 PA2 PA3	O	Output-only port PA0 to PA3 • 4-bit and single-bit output • When an input instruction is executed, the contents of the output latch are input.	• Pch: Pu MOS type • Nch: Medium sink current type • +15V breakdown voltage at Nch OD configuration	• With Pu MOS or Nch OD output	H
PB0 PB1 PB2 PB3	O	Output-only port PB0 to PB3 • 4-bit and single-bit output • When an input instruction is executed, the contents of the output latch are input.	• Pch: Pu MOS type • Nch: Medium sink current type	• With Pu MOS or Nch OD output	H
PC0 PC1 PC2/VREF0 PC3/VREF1	I/O	Input/output common port PC0 to PC3 • 4-bit and single-bit input/output • PC2: Common with VREF0 comparator comparison voltage pin • PC3: Common with VREF1 comparator comparison voltage pin	• Pch: CMOS type • Nch: Small sink current type	• CMOS or Nch OD output	H
PD0/CMP0 PD1/CMP1 PD2/CMP2 PD3/CMP3	I	Input-only port PD0 to PD3 • The comparator input is software-selectable. The comparison voltage of PD0 is VREF0. The comparison voltage of PD1 to PD3 is VREF1. The comparator is specified in units of PD0, PD1, (PD2, PD3).			Normal input
PE0/TRA PE1/TRB	I	Input-only port • The 3-level input port is software-selectable.			Normal input
OSC1 OSC2	I O	Pins for externally connecting R, C or a ceramic resonator for system clock generation. For the external clock mode, the OSC2 pin is left open and the OSC1 pin is used for input.		• Ceramic resonator OSC, RC OSC, or external clock	
RES	I	System reset input pin • When the RES is brought to L level at P33/HOLD=H, the CPU is initialized.			
TEST	I	CPU test pin Connected to VSS at the operating mode			
VDD VSS		Power supply pins			

Remarks: Output with Pu MOS ----- Output with pull-up MOS transistor
 CMOS output ----- Complementary output
 OD output ----- Open drain output

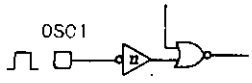
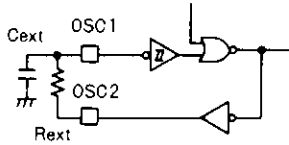
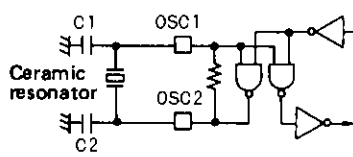
User Options

(1) Options of ports 0, 1, 8 output level during reset

For input/output ports 0, 1, 8, either of the following two output levels may be selected in a group of 4 bits during reset by option.

Option Name	Conditions, etc.
1. Output during reset: "H" level	All of 4 bits of ports 0, 1, 8
2. Output during reset: "L" level	All of 4 bits of ports 0, 1, 8

(2) Oscillator Circuit Options

Option Name	Circuit	Conditions, etc.
1. External clock		• Input: Schmitt type
2. 2-pin RC OSC		• Input: Schmitt type
3. Ceramic resonator OSC		

(3) Watchdog timer option

The presence or absence of the runaway detection function (watchdog timer) may be selected by option.

(4) Options of port output configuration

- i) For each port of P0, P1, P2, P3 (except P33/HOLD), P4, P5, P6, P7, P9, PA, PB, PC, either of the following two output configurations may be selected by option (in bit units).

Option Name	Circuit	Conditions, etc.
1. Open drain type output		P7, PA, PB: Output only P2, P3, P6, P9: Schmitt input
2. Output with pull-up resistance		P7, PA, PB: Output only P2, P3, P6, P9: Schmitt input CMOS output (P2, P3, P6, P9, PC) or Pu MOS output (P0, P1, P4, P5, P7, PA, PB) is selected according to Pch Tr drive capacity.

- ii) For P8, either of the two options may be selected (in bit units).

Option Name	Circuit	Conditions, etc.
1. Open drain output		
2. Output with pull-down resistance		

- iii) The comparator input of PD and the 3-level input of PE are software-selectable.

(1) Absolute Maximum Ratings at $T_a=25^{\circ}\text{C}$, $V_{SS}=0\text{V}$

Parameter	Symbol	Applicable Pins, Remarks	Conditions	Limits	Unit	Note
Maximum Supply Voltage	$V_{DD\text{ max}}$	VDD		$-0.3\text{ to }+7.0$	V	
Input Voltage	$V_{IN(1)}$	P2,P3(except P33/HOLD), P6		$-0.3\text{ to }+15.0$	V	1
	$V_{IN(2)}$	Other inputs		$-0.3\text{ to }V_{DD}+0.3$	V	2
Output Voltage	$V_{OUT(1)}$	P2,P3(except P33/HOLD), P6,P7,PA		$-0.3\text{ to }+15.0$	V	1
	$V_{OUT(2)}$	Other outputs		$-0.3\text{ to }V_{DD}+0.3$	V	2
Output Current per Pin	$I_{ON(1)}$	P0,P1,P2,P3(except P33/HOLD), P4,P5,P6,P8,P9, PC		4	mA	3
	$I_{ON(2)}$	P7,PA,PB		20	mA	3
	$-I_{OP(1)}$	P0,P1,P4,P5,P7,PA, PB		2	mA	4
	$-I_{OP(2)}$	P2,P3(except P33/HOLD), P6,P8,P9,PC		4	mA	4
Total Pin Current	$\Sigma I_{ON(1)}$	P2,P3(except P33/HOLD), P4,P5,P6,P7,P8		75	mA	3
	$\Sigma I_{ON(2)}$	P0,P1,P9,PA,PB,PC		75	mA	3
	$-\Sigma I_{OP(1)}$	P2,P3(except P33/HOLD), P4,P5,P6,P7,P8		25	mA	4
	$-\Sigma I_{OP(2)}$	P0,P1,P9,PA,PB,PC		25	mA	4
Allowable Power Dissipation	$P_d\text{ max}$	$T_a=-30\text{ to }+70^{\circ}\text{C}$	DIP-64S (QIP-64)	600(430)	mW	5
Operating Temperature	T_{opr}			$-30\text{ to }+70$	$^{\circ}\text{C}$	
Storage Temperature	T_{stg}			$-55\text{ to }+125$	$^{\circ}\text{C}$	

(Note 1) Applicable only when the open drain output type is selected. If other type than the open drain output is selected, the specification indicated in the column for other pins applies.

(Note 2) For OSC input/output, up to self OSC level is allowable.

(Note 3) Sink current (applicable to P8 only when the CMOS output type is selected)

(Note 4) Source current (applicable to pins other than P8 only when the pull-up output type or CMOS output type is selected)

(Note 5) Reflow soldering is recommended for QIP packages.

Please consult your local representative for information on solder-bath immersion of the device.

(2) Allowable Operating Conditions at $T_a=-30\text{ to }+70^{\circ}\text{C}$, $V_{SS}=0\text{V}$ unless otherwise specified

Parameter	Symbol	Applicable Pins	Conditions	Limits				Unit	Note
				VDD(V)	min	typ	max		
Operating Voltage	VDD	VDD			4.0	5.0	6.0	V	
Data Retention Voltage	VDD(H)	VDD	HOLD mode		1.8		6.0	V	
“H”-Level Input Voltage	VIH(1)	P2,P3(except P33/HOLD), P6	Output Nch Tr OFF	4.0to6.0	0.75VDD		+13.5	V	1
	VIH(2)	P33/HOLD,P9, RES OSC1	Output Nch Tr OFF	4.0to6.0	0.75VDD		VDD	V	2
	VIH(3)	P0,P1,P4,P5,PC, PD,PE	Output Nch Tr OFF	4.0to6.0	0.7VDD		VDD	V	3
	VIH(4)	PE	3-level input mode	4.0to6.0	0.8VDD		VDD	V	

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Parameter		Symbol	Applicable Pins	Conditions	Limits			Unit	Note			
					VDD(V)	min	typ			max		
"M"-Level Input Voltage		VIM	PE	3-level input mode	4.0to6.0	0.4VDD		0.6VDD	V			
Common-Mode Input Voltage Range		VCOMM	PD, PC2, PC3	Comparator input mode	4.0to6.0	1.0		VDD-1.5	V			
"L"-Level Input Voltage		VIL(1)	P2,P3(except P33/ HOLD), P6,P9, RES	Output Nch Tr OFF	4.0to6.0	VSS		0.25VDD	V	2		
			OSC1									
		VIL(2)	P33/HOLD		1.8 to6.0	VSS		0.25VDD	V			
		VIL(3)	P0, P1, P4, P5, PC, PD, PE, TEST	Output Nch Tr OFF	4.0to6.0	VSS		0.3VDD	V	3		
		VIL(4)	PE	3-level input mode	4.0to6.0	VSS		0.2VDD	V			
Operating Frequency (Instruction Cycle Time)		fOP (TCYC)			4.0to6.0	0.4 (10)		4.35 (0.92)	MHz (μs)			
External Clock Input Conditions	Frequency	fext	OSC1	See Fig. 1. The OSC1 is used for input and the OSC2 is left open. (OSC option: External clock input)	4.0to6.0	0.4		4.35	MHz			
	Pulse Width	textH textL		See Fig. 1. The OSC1 is used for input and the OSC2 is left open. (OSC option: External clock input)	4.0to6.0	70			ns			
	Rise/Fall Time	textR textF		See Fig. 1. The OSC1 is used for input and the OSC2 is left open. (OSC option: External clock input)	4.0to6.0			30	ns			
Self OSC Conditions	Ceramic Resonator OSC	OSC Frequency	fCF	OSC1, OSC2	See Fig. 2.	4MHz	4.0to6.0		4.0		MHz	
		OSC Stabilizing Period	tCFS		Fig. 3	4MHz	4.0to6.0			10		ms
	External Constants for RC OSC		Cext Rext	OSC1, OSC2	See Fig. 4.	4.0to6.0			100 2.7		pF kΩ	

(Note 1) Applicable to pins of open drain type. For P33/HOLD, V_{IL}(2) applies.

P2, P3, P6 of CMOS output type cannot be used as input pin.

(Note 2) Applicable to pins of open drain type. P9 of CMOS output type cannot be used as input pin.

(Note 3) When PE is used for 3-level input, V_{IL}(4), V_{IM}, V_{IL}(4) apply. PC of CMOS output type cannot be used as input pin.

LC66512B, 66516B

(3) Electrical Characteristics at Ta=-30 to +70°C, VSS=0V unless otherwise specified

Parameter	Symbol	Applicable Pins	Conditions	VDD (V)	Limits			Unit	Note
					min	typ	max		
"H"-Level Input Current	I _{IH} (1)	P2, P3 (except P33/HOLD), P6	V _{IN} =13.5V Output Nch Tr OFF	4.0 to 6.0			5.0	μA	1
	I _{IH} (2)	P0, P1, P4, P5, P9, PC, OSC1, $\overline{\text{RES}}$, P33/HOLD (except PD, PE, PC2, PC3)	V _{IN} =VDD Output Nch Tr OFF	4.0 to 6.0			1.0	μA	1
	I _{IH} (3)	PD, PE, PC2, PC3	V _{IN} =VDD Output Nch Tr OFF	4.0 to 6.0			1.0	μA	1
"L"-Level Input Current	I _{IL} (1)	Inputs other than PD, PE, PC2, PC3	V _{IN} =VSS Output Nch Tr OFF	4.0 to 6.0	-1.0			μA	2
	I _{IL} (2)	PC2, PC3, PD, PE	V _{IN} =VSS Output Nch Tr OFF	4.0 to 6.0	-1.0			μA	2
"H"-Level Output Voltage	VOH(1)	P2, P3 (except P33/HOLD), P6, P8, P9, PC	I _{OH} =-1mA	4.0 to 6.0	VDD-1.0			V	3
			I _{OH} =-0.1mA	4.0 to 6.0	VDD-0.5			V	3
	VOH(2)	P0, P1, P4, P5, P7, PA, PB	I _{OH} =-200μA	4.5	2.4			V	4
			I _{OH} =-130μA	4.5 to 5.5	VDD-1.35			V	4
Output Pull-up Current	I _{PO}	P0, P1, P4, P5, P7, PA, PB	V _{IN} =VSS	6.0	-1.6			mA	4
"L"-Level Output Voltage	VOL(1)	P0, P1, P2, P3, P4, P5, P6, P8, P9, PC (except P33/HOLD)	I _{OL} =1.6mA	4.0 to 6.0			0.4	V	5
	VOL(2)	P7, PA, PB	I _{OL} =10mA	4.0 to 6.0			1.5	V	
Output OFF-State Leakage Current	I _{OFF} (1)	P2, P3, P6, P7, PA	V _{IN} =13.5V	4.0 to 6.0			5.0	μA	6
	I _{OFF} (2)	(Except P2, P3, P6, P7, P8, PA)	V _{IN} =VDD	4.0 to 6.0			1.0	μA	6
	I _{OFF} (3)	P8	V _{IN} =VSS	4.0 to 6.0	-1.0			μA	7
Comparator Offset Voltage	V _{OFF}	PD	V _{IN} =1.0V to VDD-1.5V	4.0 to 6.0		±50	±300	mV	
Schmitt Characteristics	Hysteresis Voltage	P2, P3, $\overline{\text{RES}}$, P6, P9, OSC1 (RC, EXT)		4.0 to 6.0		0.1VDD		V	
	"H"-Level Threshold Voltage				0.5VDD		0.75VDD	V	
	"L"-Level Threshold Voltage				0.25VDD		0.5VDD	V	
RC OSC Frequency	f _{RC}	OSC1, OSC2	See Fig. 4 C=100pF±5% R=2.7kΩ±1%	4.0 to 6.0	2.0	3.0	4.0	MHz	

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Parameter		Symbol	Applicable Pins		Conditions	VDD(V)	Limits			Unit	Note
Serial Clock	Cycle Time	Input	tCKCY	SCK0, SCK1	Timing of Fig. 5 and test load of Fig. 6.	4.0 to 6.0	0.9			μ S	
		Out-put				4.0 to 6.0	2.0			TCYC	
	"L"/"H". Level Pulse Width	Input				4.0 to 6.0	0.4			μ S	
		Out-put				4.0 to 6.0	1.0			TCYC	
	Rise/Fall Time	Output				4.0 to 6.0			0.1	μ S	
Serial Input	Data Setup Time	tICK	SIO, SII		Timing of Fig. 5, specified for SCK0, SCK1 rise (↑)	4.0 to 6.0	0.3			μ S	
	Data Hold Time	tCKI				4.0 to 6.0	0.3			μ S	
Serial Output	Output Delay Time	tCKO	S00, S01		Timing of Fig. 5 and test load of Fig. 6, specified for SCK0, SCK1 fall (↓)	4.0 to 6.0			0.3	μ S	
Pulse Input Conditions	"H"/"L". Level Pulse Width at INT0	tIOH tIOL	INT0	Fig. 7.	• Condition under which the INT0 interrupt is accepted • Condition under which the event counter/pulse width measure input by timer 0 is accepted	4.0 to 6.0	2			TCYC	
	Interrupt Input "H"/"L". Level Pulse Width at Other than INT0	tIIH tIIL	INT1, INT2 INT3, INT4 INT5				2			TCYC	
	"H"/"L". Level Pulse Width at PIN1	tPINH tPINL	PIN1				2			TCYC	
	"H"/"L". Level Pulse Width at RES	tRSH tRSL	RES				3			TCYC	
Comparator Response Time	TRS	PD		Fig. 8.		4.0 to 6.0			30	μ S	
Current Dissipation at Operating Mode	IDD op	VDD			4MHz ceramic resonator OSC	4.0 to 6.0		4.5	8	mA	8
					4MHz external clock			6.5	11	mA	
					RC OSC			4.0	8	mA	

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Applicable Pins	Conditions	VDD(V)	Limits			Unit	Note
					min	typ	max		
Current Dissipation at HALT Mode	IDDHALT	VDD	4MHz ceramic resonator OSC	4.0 to 6.0		1.0	2.5	mA	
			4MHz external clock			2	3.5	mA	
			RC OSC			1.2	2.5	mA	
Current Dissipation at HOLD Mode	IDDHOLD	VDD		1.8 to 6.0		0.01	10	μA	

- (Note 1) The input/output common ports are of open drain output type with output transistor OFF. When the CMOS output type is selected, the input/output common ports cannot be used as the input pins.
- (Note 2) The input/output common ports are of open drain output type with output transistor OFF. The specification for pull-up output type is specified by output pull-up current IPO. When CMOS output type is selected, the input/output common ports cannot be used as the input pins.
- (Note 3) CMOS output type and output Nch transistor OFF (The open drain type can be also selected for P8.)
- (Note 4) Pull-up output type and output Nch transistor OFF.
- (Note 5) P8 is of CMOS output type.
- (Note 6) Open drain output type and output Nch transistor OFF.
- (Note 7) Open drain output type and output Pch transistor OFF.
- (Note 8) Reset mode.

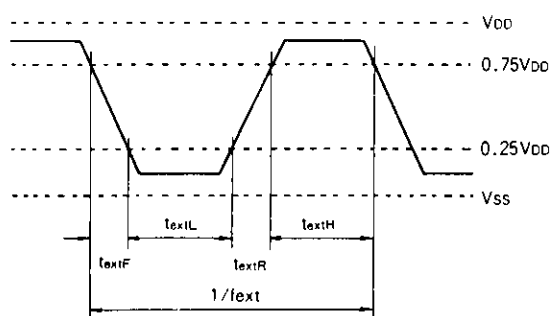
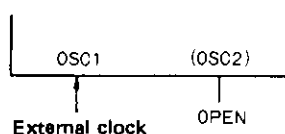


Fig. 1 External Clock Input Waveform

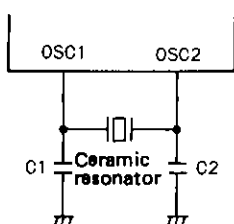


Fig. 2 Ceramic Resonator OSC Circuit

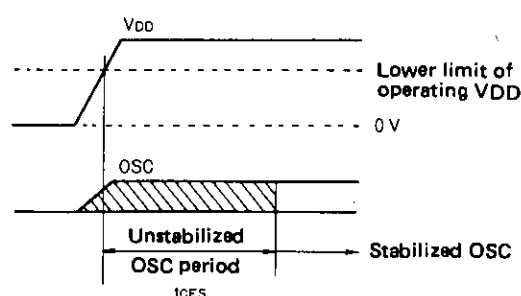


Fig. 3 OSC Stabilizing Period

External capacitor type	4 MHz (Murata) CSA4.00MG	C1	33pF ± 10%
		C2	33pF ± 10%
	4 MHz (Kyocera) KBR4.0MS	C1	33pF ± 10%
		C2	33pF ± 10%
On-chip capacitor type	4 MHz (Murata) CST4.00MG		
	4 MHz (kyocera) KBR-4.0MES		

Table 1 Ceramic Resonator OSC-Guaranteed Constants

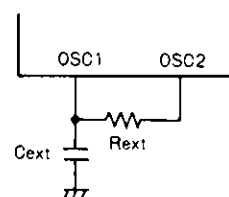


Fig. 4 RC OSC

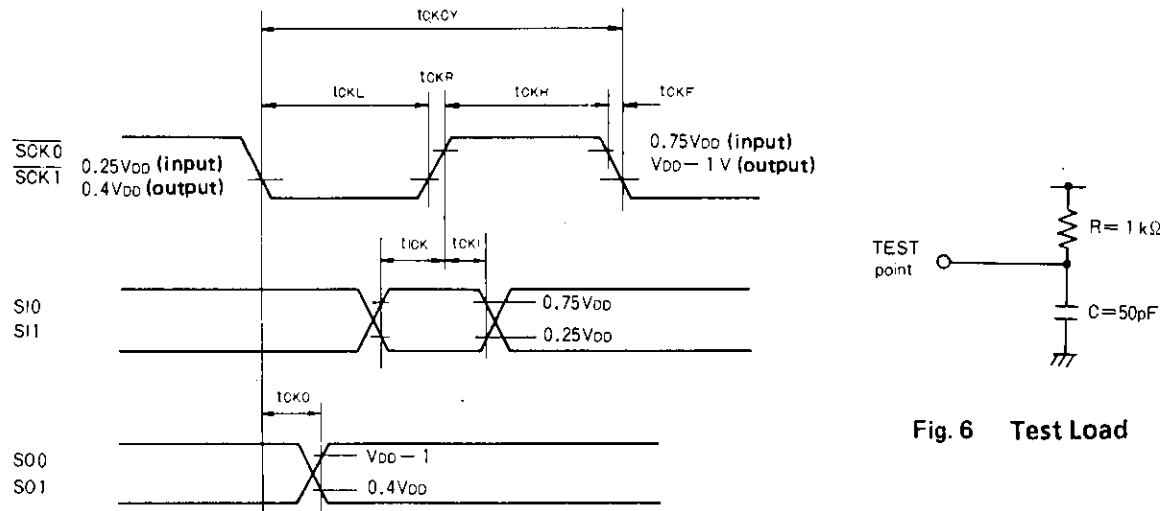


Fig. 5 Serial Input/Output Timing

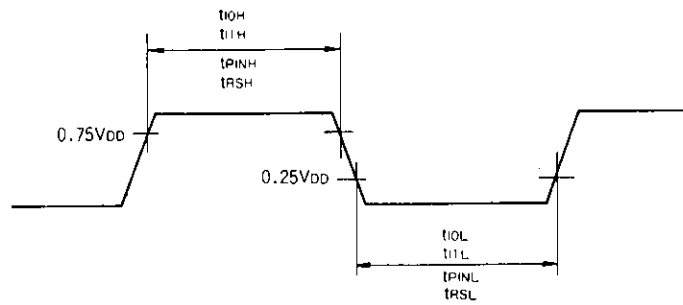


Fig. 7 $\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{INT5}$, $\overline{PIN1}$, $\overline{RES}$ Input Timing

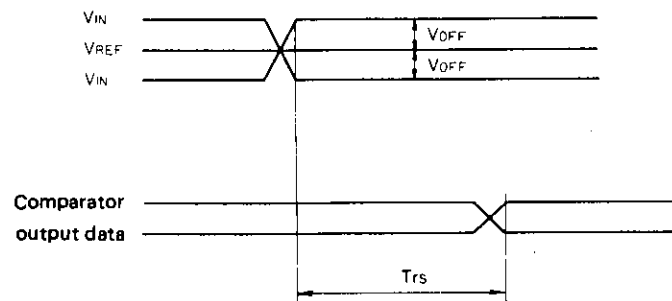


Fig. 8 Timing of Comparator Response Time T_{rs}

RC OSC Characteristic of the LC66512B, 66516B

Fig. 9 shows the RC OSC characteristic of the LC66512B, 66516B. For the variation range of RC OSC frequency of the LC66512B, 66516B, the following are guaranteed at the external constants only shown below.

External constants $C_{ext}=100\text{pF}$, $R_{ext}=2.7\text{k}\Omega$

$2.0\text{MHz} \leq f_{RC} \leq 4.0\text{MHz}$ ($T_a = -30^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD}=4.0$ to 6.0V)

If any other constants than specified above are used, the range of $R_{ext}=\text{T.B.Dk}\Omega$ to $\text{T.B.Dk}\Omega$, $C_{ext}=\text{T.B.DpF}$ to T.B.DpF must be observed. (See Fig. 9.)

(Note 10) The OSC frequency at $V_{DD}=4.0$ to 6.0V , $T_a = -30$ to $+70^\circ\text{C}$ must be within the operation clock frequency range (0.4 to 4.3MHz).

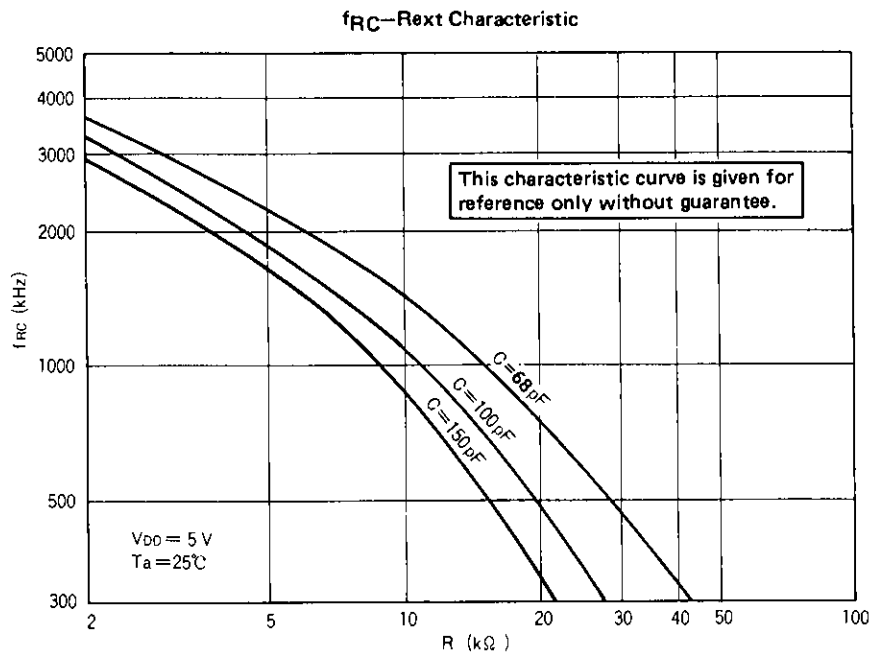
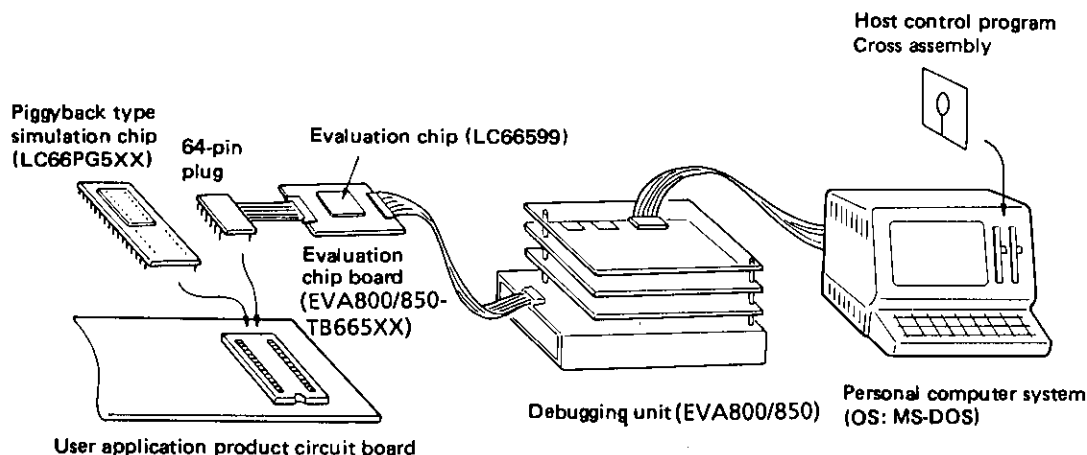


Fig. 9 RC OSC Frequency Data (Typ.)

Application Development Tools

The programs for the LC66512B, 66516B microcomputers can be developed on the MS-DOS personal computer system (IBM-PC model system). Cross assembler for this system is provided. To help the user develop programs for the LC66512B, 66516B microcomputers, the following development tools are prepared:



Appearance of Application Development Tools

(1) Program debugging unit (EVA800/850)

The program debugging unit (EVA800/850) is an emulator that includes the EPROM WRITE function and the parallel/serial data communications interface function between the unit itself and external systems (host computer, etc.). Application programs can be developed, corrected, and debugged at the machine language level. The debugging function can be carried out through break, step and trace operations. (Use the MPM665XX as the monitor ROM on the EVA800/850 debugging unit.)

(2) Evaluation chip board (EVA800/850-TB665XX)

The evaluation chip board sends control signals to the user application board through the 64-pin connector. Data is transferred between the I/O ports on the evaluation chip board and the user application board through the 64-pin connector. If the LC66599 evaluation chip is connected to the 64-pin plug by the output cable, the data from the LC66599 microcomputer is converted into the LC66506B, 66508B-bound data by the plug. There are jumper connectors on the evaluation chip board. They are used to select options and status levels. Therefore, using these jumper connectors, the same input/output formats and functions as those of the LC66506B, 66508B microcomputers can be selected on the evaluation chip board.

Jumpers

Type	OSC		Reset type selection		Power supply to the user application board through the evaluation chip board	
Jumper name	Jumper 1 (J1)		Jumper 2 (J2)		Jumper 3 (J3)	
Jumper setting and mode	EXT	External clock	INT	Reset by the RUN instruction from the host computer.	ON	VDD supply to the user application board through the evaluation chip board output.
	RC	RC OSC				
	CF	Ceramic resonator OSC	EXT	Reset by the reset circuit on the user application board	OFF	Power supply to the user application board from an independent power source (from the evaluation chip board)

Switch 1 (SW1)

Type	Output level selection for ports 0,1,8 at the reset						On-chip RAM capacity selection		Watchdog timer function selection	
Switch name	POS		P1S		P8S		RC0	RC1	Capacity	WDC
Switch setting and mode	ON	Port 0 "H"	ON	Port 1 "H"	ON	Port 8 "H"	OPEN	OPEN	RESERVE	ON
							ON	OPEN	RESERVE	Watchdog timer function selected
	OPEN	Port 0 "L"	OPEN	Port 0 "L"	OPEN	Port 8 "L"	OPEN	ON	512W	OPEN
							ON	ON	512W	Watchdog timer function not selected

Switches SW2 to SW14: Pull-up resistor option select

- ① Set to ON when on-chip pull-up resistor is used. Set to OPEN when open drain output type is selected.
- ② Selectable for each pin.

LC66512B, 66516B

(3) Cross assembler

Cross assembler name (File name)	Target machine	Restriction on program development and difference in function
LC66512. EXE	LC66512B (LC66599)	Program ROM=12K bytes RAM=512x4 bits
LC66516. EXE	LC66516B (LC66599)	Program ROM=16K bytes RAM=512x4 bits

(4) Simulation chip

The simulation chip (LC66PG5XX) is a piggyback type microcomputer. An EPROM containing programs is mounted on this chip. Then, the simulation chip is incorporated into an application product board and actual operation can be monitored.

① External view and EPROM

The pin assignment and dimensions of the LC66PG5XX are the same as those of the LC66512B, 66516B. The pin assignment is shown below. The EPROM to be mountable is 27128.

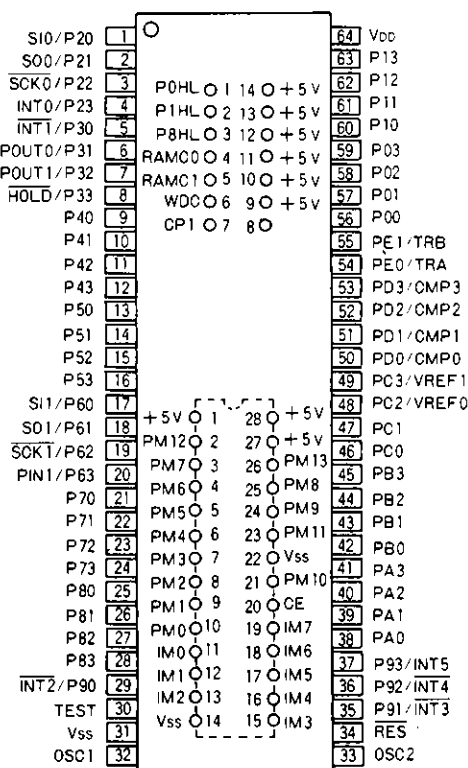
② Reset output level of ports 0, 1, 8, watchdog timer function, and memory capacity selection

Select the reset output level of ports 0, 1, 8, watchdog timer function, and memory capacity according to a microcomputer to be evaluated. Set as shown below pins 1 to 6 of the 14-pin socket on the package surface.

Function type	Pin No.	Pin name	Pin setting		Function mode
Port 0, port 1, and port 8 output level at reset	1	P0HL	ON		Port output “H”
	2	P1HL	OFF		Port output “L”
	3	P8HL			
Watchdog timer	6	WDC	ON		Operation
			OFF		Halt
On-chip RAM capacity	4	RAMC0	Pin setting		RAM capacity
	5	RAMC1	RAMC1	RAMC0	reserve
			OFF	OFF	
			OFF	ON	
			ON	OFF	512W
			ON	ON	

ON: +5V voltage input OFF: Open

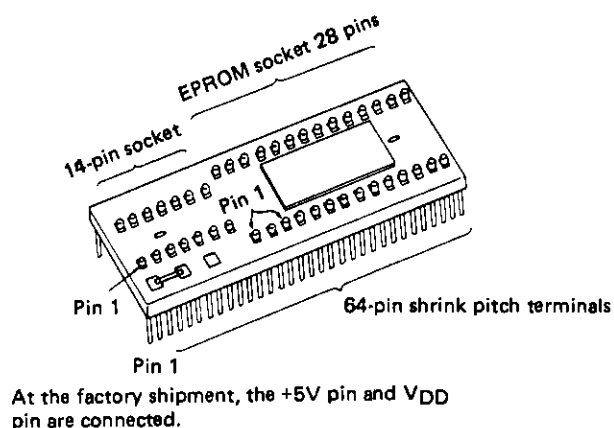
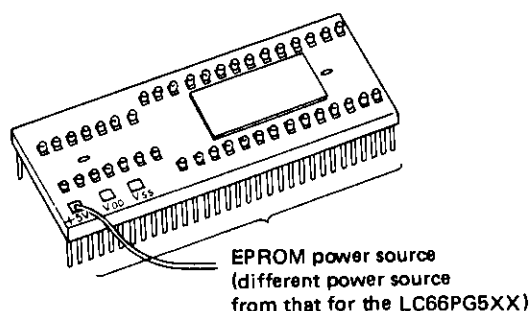
LC66PG5XX Pin Assignment



③ Power source for EPROM

Normal current dissipation per EPROM is in the range of 50mA to 100mA. When power capacity of an application product is not sufficient, power can be supplied to the EPROM from external independent power source. That is, the power source which is different from that on the application system can be selected. (See the figure given below.)

At the factory shipment, the +5V pin and V_{DD} pin are connected on the LC66PG5XX. Therefore, power is supplied to the EPROM from the LC66PG5XX power source terminal. Of the power source pads on the package surface, +5V pad is used to supply power to the EPROM.



The LC66E516 microcontroller with built-in EPROM and LC66P516 microcontroller with built-in one-time programmable ROM are used as emulation chips for the LC66506B and LC66508B.

Data sheets for the emulation chips are in preparation.

Please contact your local representative for further information.

LC665XX SERIES INSTRUCTION SET (BY FUNCTION)

Symbol	Description
AC	: Accumulator
E	: E register
CF	: Carry flag
ZF	: Zero flag
HL	: Data pointer DPH, DPL
XY	: Data pointer DPX, DPY
M	: Data memory
M (HL)	: Data memory contents specified by data pointer DPH, DPL
M (XY)	: Data memory contents specified by supplementary data pointer DPX, DPY
M2 (HL)	: 2-word data memory contents specified by data pointer DPH, DPL. In this case, the accessed data memory area address must be multiples of 2 (even address).
SP	: Stack pointer
M2 (SP)	: 2-word data memory contents specified by stack pointer
M4 (SP)	: 4-word data memory contents specified by stack pointer
in	: n-bit immediate data
t2	: Bit specification

t2	11	10	01	00
Bit	2^3	2^2	2^1	2^0

PCh	: Bits 8 to 11 of PC
PCm	: Bits 4 to 7 of PC
PCl	: Bits 0 to 3 of PC
Fn	: User's flag n=0 to 15
TIMER0	: Timer 0
TIMER1	: Timer 1
SIO	: Serial register
P	: Port
P (i4)	: Port contents specified by 4-bit immediate data
INT	: Interrupt enable flag
(), []	: Contents
←	: Transfer direction and operation result
⊕	: Exclusive logical sum
∧	: Logical product
∨	: Logical sum
+	: Addition
−	: Subtraction
—	: 1's complement

Instruction type	Mnemonics		Instruction code		Bytes	Cycles	Function	Description	Status flags affected	Remarks
			D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀						
Accumulator manipulation instructions	CLA	Clear AC	1 0 0 0	0 0 0 0	1	1	AC ← 0 (Equivalent to LAI 0)	Clears AC.	ZF	Only the first instruction is effective if executed continuously (skip function).
	DAA	Decimal adjust AC in addition	1 1 0 0 0 0 1 0	1 1 1 1 0 1 1 0	2	2	AC ← (AC) + 6 (Equivalent to ADI 6)	Adds 6 to AC.	ZF	
	DAS	Decimal adjust AC in subtraction	1 1 0 0 0 0 1 0	1 1 1 1 1 0 1 0	2	2	AC ← (AC) + 10 (Equivalent to ADI 0AH)	Adds 10 to AC.	ZF	
	CLC	Clear CF	0 0 0 1	1 1 1 0	1	1	CF ← 0	Clears CF.	CF	
	STC	Set CF	0 0 0 1	1 1 1 1	1	1	CF ← 1	Sets CF.	CF	
	CMA	Complement AC	0 0 0 1	1 0 0 0	1	1	AC ← (AC)	Gives 1's complement of (invert) AC.	ZF	
	IA	Increment AC	0 0 0 1	0 1 0 0	1	1	AC ← (AC) + 1	Adds 1 to AC.	ZF, CF	
	DA	Decrement AC	0 0 1 0	0 1 0 0	1	1	AC ← (AC) - 1	Subtracts 1 from AC.	ZF, CF	
	RAR	Rotate AC right through CF	0 0 0 1	0 0 0 0	1	1	AC ₀ ← (CF), AC _n ← (AC _{n+1}), CF ← (AC ₀)	Rotates AC right through CF.	CF	
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC ₀ ← (CF), AC _{n+1} ← (AC _n), CF ← (AC ₀)	Rotates AC left through CF.	CF, ZF	
	TAE	Transfer AC to E	0 1 0 0	0 1 0 1	1	1	E ← (AC)	Transfers the AC contents to the E register.		
	TEA	Transfer E to AC	0 1 0 0	0 1 1 0	1	1	AC ← (E)	Transfers the E register contents to AC.	ZF	
Memory manipulation instructions	XAE	Exchange AC with E	0 1 0 0	0 1 0 0	1	1	(AC) ↔ (E)	Exchanges the contents of the AC and E register.		
	IM	Increment M	0 0 0 1	0 0 1 0	1	1	M(HL) ← (M(HL)) + 1	Adds 1 to M(HL).	ZF, CF	
	DM	Decrement M	0 0 1 0	0 0 1 0	1	1	M(HL) ← (M(HL)) - 1	Subtracts 1 from M(HL).	ZF, CF	
	IMDR i8	Increment M direct	1 1 0 0 i ₇ i ₆ i ₅ i ₄	0 1 1 1 i ₃ i ₂ i ₁ i ₀	2	2	M(i8) ← (M(i8)) + 1	Adds 1 to M(i8).	ZF, CF	
	DMDR i8	Decrement M direct	1 1 0 0 i ₇ i ₆ i ₅ i ₄	0 0 1 1 i ₃ i ₂ i ₁ i ₀	2	2	M(i8) ← (M(i8)) - 1	Subtracts 1 from M(i8).	ZF, CF	
	SMB t2	Set M data bit	0 0 0 0	1 1 t ₁ t ₀	1	1	(M(HL), t2) ← 1	Sets a bit specified by t1t0 of M(HL).		
Operation/Comparison instructions	RMB t2	Reset M data bit	0 0 1 0	1 1 t ₁ t ₀	1	1	(M(HL), t2) ← 0	Resets a bit specified by t1t0 of M(HL).	ZF	
	AD	Add M to AC	0 0 0 0	0 1 1 0	1	1	AC ← (AC) + (M(HL))	Adds together the contents of AC and M(HL) in binary and stores the result in AC.	ZF, CF	
	ADDR i8	Add M direct to AC	1 1 0 0 i ₇ i ₆ i ₅ i ₄	1 0 0 1 i ₃ i ₂ i ₁ i ₀	2	2	AC ← (AC) + (M(i8))	Adds together the contents of AC and M(i8) in binary and stores the result in AC.	ZF, CF	
	ADC	Add M to AC with CF	0 0 0 0	0 0 1 0	1	1	AC ← (AC) + (M(HL)) + (CF)	Adds together the contents of AC, M(HL), and CF in binary and stores the result in AC.	ZF, CF	
	ADI i4	Add immediate data to AC	1 1 0 0 0 0 1 0	1 1 1 1 i ₃ i ₂ i ₁ i ₀	2	2	AC ← (AC) + i ₃ i ₂ i ₁ i ₀	Adds together the contents of AC and immediate data in binary and stores the result in AC.	ZF	
	SUBC	Subtract AC from M with CF	0 0 0 1	0 1 1 1	1	1	AC ← (M(HL)) - (AC) - (CF)	Subtracts the contents of AC from M(HL) with CF in binary and stores the result in AC.	ZF, CF	CF=0 if there is a borrow while CF=1 if there is no borrow.
	ANDA	AND M with AC then store AC	0 0 0 0	0 1 1 1	1	1	AC ← (AC) ∧ (M(HL))	Performs a logical AND operation between AC and M(HL) and stores the result in AC.	ZF	
	ORA	OR M with AC then store AC	0 0 0 0	0 1 0 1	1	1	AC ← (AC) ∨ (M(HL))	Performs a logical OR operation between AC and M(HL) and stores the result in AC.	ZF	
	EXL	Exclusive OR M with AC then store AC	0 0 0 1	0 1 0 1	1	1	AC ← (AC) ⊕ (M(HL))	Performs a logical exclusive OR operation between AC and M(HL) and stores the result in AC.	ZF	
	ANDM	AND M with AC then store M	0 0 0 0	0 0 1 1	1	1	M(HL) ← (AC) ∧ (M(HL))	Performs a logical AND operation between AC and M(HL) and stores the result in M(HL).	ZF	
	ORM	OR M with AC then store M	0 0 0 0	0 1 0 0	1	1	M(HL) ← (AC) ∨ (M(HL))	Performs a logical OR operation between AC and M(HL) and stores the result in M(HL).	ZF	

Instruction type	Mnemonics	Instruction code		Bytes	Cycles	Function	Description	Status flags affected	Remarks												
		D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀																		
Operation/Comparison instructions	CM	Compare AC with M	0 0 0 1 0 1 1 0	1	1	$[M(HL)] + (AC) + 1$	Compares the contents of AC and M(HL) and then sets/resets the carry flag (CF) and zero flag (ZF). <table><tr><th>Comparison relations</th><th>CF</th><th>ZF</th></tr><tr><td>$[M(HL)] > (AC)$</td><td>0</td><td>0</td></tr><tr><td>$[M(HL)] = (AC)$</td><td>1</td><td>1</td></tr><tr><td>$[M(HL)] < (AC)$</td><td>1</td><td>0</td></tr></table>	Comparison relations	CF	ZF	$[M(HL)] > (AC)$	0	0	$[M(HL)] = (AC)$	1	1	$[M(HL)] < (AC)$	1	0	ZF, CF	
	Comparison relations	CF	ZF																		
	$[M(HL)] > (AC)$	0	0																		
	$[M(HL)] = (AC)$	1	1																		
$[M(HL)] < (AC)$	1	0																			
CI i4	Compare AC with immediate data	1 1 0 0 1 1 1 1 1 0 1 0 i ₃ i ₂ i ₁ i ₀	2	2	$i_3 i_2 i_1 i_0 + (AC) + 1$	Compares the contents of the accumulator (AC) and immediate data i ₃ i ₂ i ₁ i ₀ and sets/resets the zero flag (ZF) and carry flag (CF). <table><tr><th>Comparison relations</th><th>CF</th><th>ZF</th></tr><tr><td>$i_3 i_2 i_1 i_0 > AC$</td><td>0</td><td>0</td></tr><tr><td>$i_3 i_2 i_1 i_0 = AC$</td><td>1</td><td>1</td></tr><tr><td>$i_3 i_2 i_1 i_0 < AC$</td><td>1</td><td>0</td></tr></table>	Comparison relations	CF	ZF	$i_3 i_2 i_1 i_0 > AC$	0	0	$i_3 i_2 i_1 i_0 = AC$	1	1	$i_3 i_2 i_1 i_0 < AC$	1	0	ZF, CF		
Comparison relations	CF	ZF																			
$i_3 i_2 i_1 i_0 > AC$	0	0																			
$i_3 i_2 i_1 i_0 = AC$	1	1																			
$i_3 i_2 i_1 i_0 < AC$	1	0																			
CLI i4	Compare DPL with immediate data	1 1 0 0 1 1 1 1 1 0 1 1 i ₃ i ₂ i ₁ i ₀	2	2	ZF ← 1 if (DPL) = i ₃ i ₂ i ₁ i ₀ ZF ← 0 if (DPL) ≠ i ₃ i ₂ i ₁ i ₀	Compares the contents of DPL and immediate data and sets the zero flag (ZF) if they are equal, or resets the flag if not equal.	ZF														
CMB i2	Compare AC bit with M data bit	1 1 0 0 1 1 1 1 1 1 0 1 0 0 t ₁ t ₀	2	2	ZF ← 1 if (AC, t ₂) = (M(HL), t ₂) ZF ← 0 if (AC, t ₂) ≠ (M(HL), t ₂)	Compares the contents of AC and M(HL) bit specified by the 2 bits (t ₁ and t ₂) of the instruction and sets the zero flag (ZF) if they are equal, or resets the flag if not equal.	ZF														
Load/store instructions	LAE	Load AC and E from M2 (HL)	0 1 0 1 1 1 0 0	1	1	AC ← M(HL) E ← M(HL + 1)	Loads the contents of M2(HL) into the AC and the E register.														
	LAI i4	Load AC with immediate data	1 0 0 0 i ₃ i ₂ i ₁ i ₀	1	1	AC ← i ₃ i ₂ i ₁ i ₀	Loads immediate data into AC.	ZF	Only the first instruction is effective if executed continuously (skip function).												
	LADR i8	Load AC from M direct	1 1 0 0 0 0 0 1 i ₇ i ₆ i ₅ i ₄ i ₃ i ₂ i ₁ i ₀	2	2	AC ← [M(i8)]	Loads the contents of M(i8) into AC.	ZF													
	S	Store AC to M	0 1 0 0 0 1 1 1	1	1	M(HL) ← (AC)	Stores the contents of AC into M(HL).														
	SAE	Store AC and E to M2 (HL)	0 1 0 1 1 1 1 0	1	1	M(HL) ← (AC) M(HL + 1) ← (E)	Stores the contents of AC and the E register into M2(HL).														
	LA reg	Load AC from M(reg)	0 1 0 0 1 0 t ₀ 0	1	1	AC ← [M(reg)]	Loads the contents of M(reg) into AC. reg is either an HL or XY. <table><tr><th>reg</th><th>to</th></tr><tr><td>HL</td><td>0</td></tr><tr><td>XY</td><td>1</td></tr></table>	reg	to	HL	0	XY	1	ZF							
	reg	to																			
	HL	0																			
	XY	1																			
	LA reg, i	Load AC from M(reg) then increment reg	0 1 0 0 1 0 t ₀ 1	1	2	AC ← [M(reg)] DPL ← (DPL) + 1 or DPY ← (DPY) + 1	Loads the contents of M(reg) into the accumulator (AC). reg is either an HL or XY. After loading, increments the contents of DPL or DPY. Refer to the LA reg instruction for the relationship between reg and t ₀ .	ZF	ZF status depends on DPL or DPY increment result.												
	LA reg, D	Load AC from M(reg) then decrement reg	0 1 0 1 1 0 t ₀ 1	1	2	AC ← [M(reg)] DPL ← (DPL) - 1 or DPY ← (DPY) - 1	Loads the contents of M(reg) into AC. reg is either an HL or XY. After loading, decrements the contents of DPL or DPY. Refer to the LA reg instruction for the relationship between reg and t ₀ .	ZF	ZF status depends on DPL or DPY decrement result.												
	XA reg	Exchange AC with M (reg)	0 1 0 0 1 1 t ₀ 0	1	1	(AC) ↔ [M(reg)]	Exchanges the contents of AC and M(reg). reg is either an HL or XY. <table><tr><th>reg</th><th>to</th></tr><tr><td>HL</td><td>0</td></tr><tr><td>XY</td><td>1</td></tr></table>	reg	to	HL	0	XY	1								
reg	to																				
HL	0																				
XY	1																				
XA reg, i	Exchange AC with M (reg) then increment reg	0 1 0 0 1 1 t ₀ 1	1	2	(AC) ↔ [M(reg)] DPL ← (DPL) + 1 or DPY ← (DPY) + 1	Exchanges the contents of AC and M(reg). reg is either an HL or XY. After exchanging, increments the contents of DPL or DPY. Refer to the XA reg instruction for the relationship between reg and t ₀ .	ZF	ZF status depends on DPL or DPY increment result.													
XA reg, D	Exchange AC with M (reg) then decrement reg	0 1 0 1 1 1 t ₀ 1	1	2	(AC) ↔ [M(reg)] DPL ← (DPL) - 1 or DPY ← (DPY) - 1	Exchanges the contents of AC and M(reg). reg is either an HL or XY. After exchanging, decrements the contents of DPL or DPY. Refer to the XA reg instruction for the relationship between reg and t ₀ .	ZF	ZF status depends on DPL or DPY decrement result.													
	XADR i8	Exchange AC with M direct	1 1 0 0 1 0 0 0 i ₇ i ₆ i ₅ i ₄ i ₃ i ₂ i ₁ i ₀	2	2	(AC) ↔ [M(i8)]	Exchanges the contents of AC and M(i8).														

Instruction type	Mnemonics	Instruction code		Bytes	Cycles	Function	Description	Status flags affected	Remarks
		D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀						
Load/store instructions	LEAI i8	Load E & AC with immediate data	1 1 0 0 i ₇ i ₆ i ₅ i ₄	0 1 1 0 i ₃ i ₂ i ₁ i ₀	2	2	E ← i ₇ i ₆ i ₅ i ₄ AC ← i ₃ i ₂ i ₁ i ₀	Loads immediate data i8 into the E register and the accumulator (AC).	
	RTBL	Read table data from program ROM	0 1 0 1	1 0 1 0	1	2	E, AC ← (ROM(PCh, E, AC))	First, replace the contents of lower 8 bits of PC with the E register and AC contents. Then, loads the ROM data at an address specified by the new contents of the lower 8 bits of PC into the E register and AC.	
	RTBLP	Read table data from program ROM then output to P4,5	0 1 0 1	1 0 0 0	1	2	Port 4, 5 ← (ROM(PCh, E, AC))	First, replaces the contents of lower 8 bits of AC with the E register and AC contents. Then, outputs the ROM data at an address specified by the new contents of the lower 8 bits of PC to ports 4 and 5.	
Data pointer manipulation instructions	LDZ i4	Load DP _H with zero and DP _L with immediate data respectively	0 1 1 0	i ₃ i ₂ i ₁ i ₀	1	1	DP _H ← 0 DP _L ← i ₃ i ₂ i ₁ i ₀	Loads the data of 0 (zero) and immediate data i4 into the DP _H and DP _L respectively.	
	LHI i4	Load DP _H with immediate data	1 1 0 0 0 0 0 0	1 1 1 1 i ₃ i ₂ i ₁ i ₀	2	2	DP _H ← i ₃ i ₂ i ₁ i ₀	Loads immediate data i4 into the DP _H .	
	LLI i4	Load DP _L with immediate data	1 1 0 0 0 0 0 1	1 1 1 1 i ₃ i ₂ i ₁ i ₀	2	2	DP _L ← i ₃ i ₂ i ₁ i ₀	Loads immediate data i4 into the DP _L .	
	LHLI i8	Load DP _H , DP _L with immediate data	1 1 0 0 i ₇ i ₆ i ₅ i ₄	0 0 0 0 i ₃ i ₂ i ₁ i ₀	2	2	DP _H ← i ₇ i ₆ i ₅ i ₄ DP _L ← i ₃ i ₂ i ₁ i ₀	Loads immediate data into the DP _H and DP _L .	
	LXYI i8	Load DP _X , DP _Y with immediate data	1 1 0 0 i ₇ i ₆ i ₅ i ₄	0 0 1 0 i ₃ i ₂ i ₁ i ₀	2	2	DP _X ← i ₇ i ₆ i ₅ i ₄ DP _Y ← i ₃ i ₂ i ₁ i ₀	Loads immediate data into the DP _X and DP _Y .	
	IL	Increment DP _L	0 0 0 1	0 0 0 1	1	1	DP _L ← (DP _L) + 1	Increments the contents of the DP _L by 1.	ZF
	DL	Decrement DP _L	0 0 1 0	0 0 0 1	1	1	DP _L ← (DP _L) - 1	Decrements the contents of the DP _L by 1.	ZF
	IY	Increment DP _Y	0 0 0 1	0 0 1 1	1	1	DP _Y ← (DP _Y) + 1	Increments the contents of the DP _Y by 1.	ZF
	DY	Decrement DP _Y	0 0 1 0	0 0 1 1	1	1	DP _Y ← (DP _Y) - 1	Decrements the contents of the DP _Y by 1.	ZF
	TAH	Transfer AC to DP _H	1 1 0 0 1 1 1 1	1 1 1 1 0 0 0 0	2	2	DP _H ← (AC)	Transfers the contents of the accumulator (AC) to the DP _H .	
	THA	Transfer DP _H to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 0 0	2	2	AC ← (DP _H)	Transfers the contents of the DP _H to the AC.	ZF
	XAH	Exchange AC with DP _H	0 1 0 0	0 0 0 0	1	1	(AC) ↔ (DP _H)	Exchanges the contents of the accumulator (AC) and the DP _H .	
	TAL	Transfer AC to DP _L	1 1 0 0 1 1 1 1	1 1 1 1 0 0 0 1	2	2	DP _L ← (AC)	Transfers the contents of the accumulator (AC) to the DP _L .	
	TLA	Transfer DP _L to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 0 1	2	2	AC ← (DP _L)	Transfers the contents of the DP _L to the accumulator (AC).	ZF
	XAL	Exchange AC with DP _L	0 1 0 0	0 0 0 1	1	1	(AC) ↔ (DP _L)	Exchanges the contents of the AC and DP _L .	
	TAX	Transfer AC to DP _X	1 1 0 0 1 1 1 1	1 1 1 1 0 0 1 0	2	2	DP _X ← (AC)	Transfers the contents of the accumulator (AC) to the DP _X .	
	TXA	Transfer DP _X to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 1 0	2	2	AC ← (DP _X)	Transfers the contents of DP _X to the AC.	ZF
	XAX	Exchange AC with DP _X	0 1 0 0	0 0 1 0	1	1	(AC) ↔ (DP _X)	Exchanges the contents of the AC and DP _X .	
	TAY	Transfer AC to DP _Y	1 1 0 0 1 1 1 1	1 1 1 1 0 0 1 1	2	2	DP _Y ← (AC)	Transfers the contents of the accumulator (AC) to the DP _Y .	
	TYA	Transfer DP _Y to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 1 1	2	2	AC ← (DP _Y)	Transfers the contents of the DP _Y to the AC.	ZF
	XAY	Exchange AC with DP _Y	0 1 0 0	0 0 1 1	1	1	(AC) ↔ (DP _Y)	Exchanges the contents of the accumulator (AC) and the DP _Y .	
Flag manipulation instructions	SFB n4	Set flag bit	0 1 1 1	n ₃ n ₂ n ₁ n ₀	1	1	F _n ← 1	Sets a flag specified by n4.	
	RFB n4	Reset flag bit	0 0 1 1	n ₃ n ₂ n ₁ n ₀	1	1	F _n ← 0	Resets a flag specified by n4.	ZF
Jump/subroutine instructions	JMP addr	Jump in the current bank	1 1 1 0 P ₇ P ₆ P ₅ P ₄	P ₁₁ P ₁₀ P ₉ P ₈ P ₃ P ₂ P ₁ P ₀	2	2	PC13,12 ← PC13,12 PC11~0 ← P ₁₁ ~P ₀	Jumps to an address specified by immediate data P ₁₁ ~ P ₀ in the current bank.	When executed immediately after the BANK instruction, PC12 ← PC12
	JPEA	Jump to the address stored at E and AC in the current page	0 0 1 0	0 1 1 1	1	1	PC13~PC8 ← PC13~PC8 PC7~4 ← (E) PC3~0 ← (AC)	Jumps to an address specified by the contents of the E register and accumulator (AC) which have replaced the contents of lower 8 bits of the program counter (PC).	

Instruction type	Mnemonics	Instruction code		Bytes	Cycles	Function	Description	Status flags affected	Remarks
		D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀						
Jump/subroutine instructions	CAL addr	0 1 0 1 P ₇ P ₆ P ₅ P ₄	0 P ₁₀ P ₉ P ₈ P ₃ P ₂ P ₁ P ₀	2	2	PC13~11←0 PC10←0—P ₁₀ ~P ₉ M4(SP)←(CF, ZF, PC13~0) SP←(SP)-4	Calls a subroutine.		
	CZP addr	1 0 1 0	P ₃ P ₂ P ₁ P ₀	1	2	PC13~6, PC1~0←0 PC5~2←P ₃ ~P ₀ M4(SP)←(CF, ZF, PC13~0) SP←SP-4	Calls a subroutine in page 0 of bank 0.		
	BANK	0 0 0 1	1 0 1 1	1	1		Changes memory banks and register banks.		
	PUSH reg	1 1 0 0 1 1 1 1	1 1 1 1 1 i ₁ i ₀ 0	2	2	M2(SP)←(reg) SP←(SP)-2	Stores the contents of reg into the M2(SP) and then subtracts 2 from the stack pointer (SP).		
	POP reg	1 1 0 0 1 1 1 0	1 1 1 1 1 i ₁ i ₀ 0	2	2	SP←(SP)+2 reg←(M2(SP))	Stores the contents of reg into the M2(SP) and then increments the contents of the stack pointer (SP) by 2 and loads the contents of M2 (SP) into a reg. Refer to the PUSH reg instruction for the relationship between i1i0 and reg.		
	RT	0 0 0 1	1 1 0 0	1	2	SP←(SP)+4 PC←(M4(SP))	Returns execution from a subroutine or interrupt processing routine back to the routine that called it. The contents of the carry flag (CF) and zero flag (ZF) are not returned from the stack area.		
	RTI	0 0 0 1	1 1 0 1	1	2	SP←(SP)+4 PC←(M4(SP)) CF, ZF←(M4(SP))	Returns execution from a subroutine or interrupt processing routine back to the routine that called it. The contents of the carry flag (CF) and zero flag (ZF) are returned from the stack area.	ZF, CF	
Branch instructions	BAt2 addr	1 1 0 1 P ₇ P ₆ P ₅ P ₄	0 0 t ₁ t ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC7~0←P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(AC, t2)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of AC is 1 (program branch).		
	BNAt2 addr	1 0 0 1 P ₇ P ₆ P ₅ P ₄	0 0 t ₁ t ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC7~0←P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(AC, t2)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of AC is 0 (program branch).		
	BMt2 addr	1 1 0 1 P ₇ P ₆ P ₅ P ₄	0 1 t ₁ t ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC7~0←P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(M(HL), t2)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of M(HL) is 1 (program branch).		
	BNMt2 addr	1 0 0 1 P ₇ P ₆ P ₅ P ₄	0 1 t ₁ t ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC7~0←P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(M(HL), t2)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of M(HL) is 0 (program branch).		
	BPt2 addr	1 1 0 1 P ₇ P ₆ P ₅ P ₄	1 0 t ₁ t ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC7~0←P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(P(DPL), t2)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of the port accessed by DPL is 1 (program branch).		Used to manipulate internal control registers if executed immediately after the BANK instruction. In this case, the internal control registers must be readable.
	BNPt2 addr	1 0 0 1 P ₇ P ₆ P ₅ P ₄	1 0 t ₁ t ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC7~0←P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(P(DPL), t2)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of the port accessed by DPL is 0 (program branch).		Same as above.
	BC addr	1 1 0 1 P ₇ P ₆ P ₅ P ₄	1 1 0 0 P ₃ P ₂ P ₁ P ₀	2	2	PC7~0←P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(CF)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the carry flag (CF) is 1 (program branch).		
	BNC addr	1 0 0 1 P ₇ P ₆ P ₅ P ₄	1 1 0 0 P ₃ P ₂ P ₁ P ₀	2	2	PC7~0←P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(CF)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the carry flag (CF) is 0 (program branch).		
	BZ addr	1 1 0 1 P ₇ P ₆ P ₅ P ₄	1 1 0 1 P ₃ P ₂ P ₁ P ₀	2	2	PC7~0←P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(ZF)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the zero flag (ZF) is 1 (program branch).		
	BNZ addr	1 0 0 1 P ₇ P ₆ P ₅ P ₄	1 1 0 1 P ₃ P ₂ P ₁ P ₀	2	2	PC7~0←P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(ZF)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the zero flag (ZF) is 0 (program branch).		

Instruction type	Mnemonics		Instruction code		Bytes	Cycles	Function	Description	Status flags affected	Remarks
			D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀						
Branch instructions	BFn4 addr	Branch on flag bit	1 1 1 1 P ₇ P ₆ P ₅ P ₄	n ₃ n ₂ n ₁ n ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC7←P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(Fn)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the flag specified by n3n2n1n0 is 1. The flag is one of the 16 flags.		
	BNFn4 addr	Branch on no flag bit	1 0 1 1 P ₇ P ₆ P ₅ P ₄	n ₃ n ₂ n ₁ n ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC7←P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(Fn)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the flag specified by n3n2n1n0 is 0. The flag is one of the 16 flags.		
Input/output instructions	IPO	Input port 0 to AC	0 0 1 0	0 0 0 0	1	1	AC←(P0)	Inputs the contents of port 0 to the accumulator (AC).	ZF	
	IP	Input port to AC	0 0 1 0	0 1 1 0	1	1	AC←(P(DPL))	Inputs the contents of port accessed by DPL to the accumulator (AC).	ZF	
	IPM	Input port to M	0 0 0 1	1 0 0 1	1	1	M(HL)←(P(DPL))	Inputs the contents of port accessed by DPL to the M(HL).		
	IPDR i4	Input port to AC direct	1 1 0 0 0 1 1 0	1 1 1 1 i ₃ i ₂ i ₁ i ₀	2	2	AC←(P(i4))	Inputs the contents of port accessed by i4 to the accumulator (AC).	ZF	
	IP45	Input port 4,5 to E, AC respectively	1 1 0 0 1 1 0 1	1 1 1 1 0 1 0 0	2	2	E ←(P(4)) AC←(P(5))	Inputs the contents of ports 4 and 5 to the E register and accumulator (AC) respectively.		
	OP	Output AC to port	0 0 1 0	0 1 0 1	1	1	P(DPL)←(AC)	Outputs the contents of the accumulator (AC) to a port accessed by DPL.		
	OPM	Output M to port	0 0 0 1	1 0 1 0	1	1	P(DPL)←(M(HL))	Outputs the contents of the M(HL) to a port accessed by DPL.		
	OPDR i4	Output AC to port direct	1 1 0 0 0 1 1 1	1 1 1 1 i ₃ i ₂ i ₁ i ₀	2	2	P(i4)←(AC)	Outputs the contents of the accumulator (AC) to a port accessed by i4.		
	OP45	Output E, AC to port 4,5 respectively	1 1 0 0 1 1 0 1	1 1 1 1 0 1 0 1	2	2	P(4)←(E) P(5)←(AC)	Outputs the contents of the E register and accumulator (AC) to ports 4 and 5 respectively.		
	SPB t2	Set port bit	0 0 0 0	1 0 t ₁ t ₀	1	1	(P(DPL), t2)←1	Sets a bit specified by immediate data t1t0 of a port accessed by DPL.		
	RPB t2	Reset port bit	0 0 1 0	1 0 t ₁ t ₀	1	1	(P(DPL), t2)←0	Resets a bit specified by immediate data t1t0 of a port accessed by DPL.	ZF	
	ANDPDR i4, p4	AND port with immediate data then output	1 1 0 0 i ₃ i ₂ i ₁ i ₀	0 1 0 1 P ₃ P ₂ P ₁ P ₀	2	2	P(P ₃ ~P ₀)←(P(P ₃ ~P ₀)∨i ₃ ~i ₀)	Performs a logical AND operation between the contents of a port specified by P3 to P0 and immediate data i3i2i1i0 and outputs the resulted product to the port.	ZF	
	ORPDR i4, p4	OR port with immediate data then output	1 1 0 0 i ₃ i ₂ i ₁ i ₀	0 1 0 0 P ₃ P ₂ P ₁ P ₀	2	2	P(P ₃ ~P ₀)←(P(P ₃ ~P ₀)∨i ₃ ~i ₀)	Performs a logical OR operation between the contents of a port specified by P3 to P0 and immediate data i3i2i1i0 and outputs the resulted sum to the port.	ZF	
Timer control instructions	WTTM0	Write timer 0	1 1 0 0	1 0 1 0	1	2	TIMER0←(M2(HL)), (AC)	Writes the contents of the M(HL) and the accumulator (AC) to the timer 0 reload register.		
	WTTM1	Write timer 1	1 1 0 0 1 1 1 1	1 1 1 1 0 1 0 0	2	2	TIMER1←(E), (AC)	Writes the contents of the E register and the accumulator (AC) to the timer 1 reload register.		
	RTIM0	Read timer 0	1 1 0 0	1 0 1 1	1	2	M2(HL), AC←(TIMER0)	Reads the contents of the timer 0 counter into the M2(HL) and the accumulator (AC).		
	RTIM1	Read timer 1	1 1 0 0 1 1 1 1	1 1 1 1 0 1 0 1	2	2	E, AC←(TIMER1)	Reads the contents of the timer 1 counter into the E register and the accumulator (AC).		
	START0	Start timer 0	1 1 0 0 1 1 1 0	1 1 1 1 0 1 1 0	2	2	Start timer 0 counter	Starts the timer 0 counter operation.		
	START1	Start timer 1	1 1 0 0 1 1 1 0	1 1 1 1 0 1 1 1	2	2	Start timer1 counter	Starts the timer 1 counter operation.		
	STOP0	Stop timer 0	1 1 0 0 1 1 1 1	1 1 1 1 0 1 1 0	2	2	Stop timer 0 counter	Stops the timer 0 counter operation.		
	STOP1	Stop timer 1	1 1 0 0 1 1 1 1	1 1 1 1 0 1 1 1	2	2	Stop timer1 counter	Stops the timer 1 counter operation.		

Instruction type	Mnemonics		Instruction code		Bytes	Cycles	Function	Description	Status flags affected	Remarks
			D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀						
Interrupt control instructions	MSET	Set Interrupt Master Enable Flag	1 1 0 0 0 1 0 1	1 1 0 1 0 0 0 0	2	2	MSE ← 1	Sets the interrupt master enable flag.		
	MRESET	Reset Interrupt Master Enable Flag	1 1 0 0 1 0 0 1	1 1 0 1 0 0 0 0	2	2	MSE ← 0	Resets the interrupt master enable flag.		
	EIH i4	Enable interrupt high	1 1 0 0 0 1 0 1	1 1 0 1 i ₃ i ₂ i ₁ i ₀	2	2	EDIH ← (EDIH) ∨ i4	Sets the interrupt enable flag.		
	EIL i4	Enable interrupt low	1 1 0 0 0 1 0 0	1 1 0 1 i ₃ i ₂ i ₁ i ₀	2	2	EDIL ← (EDIL) ∨ i4	Sets the interrupt enable flag.		
	DIH i4	Disable interrupt high	1 1 0 0 1 0 0 1	1 1 0 1 i ₃ i ₂ i ₁ i ₀	2	2	EDIH ← (EDIH) ∧ $\bar{i}4$	Resets the interrupt enable flag.	ZF	
	DIL i4	Disable interrupt low	1 1 0 0 1 0 0 0	1 1 0 1 i ₃ i ₂ i ₁ i ₀	2	2	EDIL ← (EDIL) ∧ $\bar{i}4$	Resets the interrupt enable flag.	ZF	
	WTSP	Write SP	1 1 0 0 1 1 0 1	1 1 1 1 1 0 1 0	2	2	SP ← (E), (AC)	Transfers the contents of the E register and accumulator (AC) to the stack area.		
	RSP	Read SP	1 1 0 0 1 1 0 1	1 1 1 1 1 0 1 1	2	2	E, AC ← (SP)	Transfers the contents of the stack area to the E register and accumulator (AC).		
Standby control instructions	HALT	HALT	1 1 0 0 1 1 0 1	1 1 1 1 1 1 1 0	2	2	HALT	Selects the HALT mode.		
	HOLD	HOLD	1 1 0 0 1 1 0 1	1 1 1 1 1 1 1 1	2	2	HOLD	Selects the HOLD mode.		
Serial I/O control instructions	STARTS	Start serial I/O	1 1 0 0 1 1 1 0	1 1 1 1 1 1 1 0	2	2	START SIO	Starts the SIO operation mode.		
	WTSIO	Write serial I/O	1 1 0 0 1 1 1 0	1 1 1 1 1 1 1 1	2	2	SIO ← (E), (AC)	Writes the contents of the E register and accumulator (AC) to the SIO register.		
	RSIO	Read serial I/O	1 1 0 0 1 1 1 1	1 1 1 1 1 1 1 1	2	2	E, AC ← (SIO)	Reads the contents of the SIO register into the E register and the accumulator (AC).		
Other instructions	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	A dummy instruction that is coded 00H and has no effect when executed. Just one machine cycle signal reaches the CPU.		
	SB i2	Select bank	1 1 0 0 1 1 0 0	1 1 1 1 0 0 i ₁ i ₀	2	2	PC13, PC12 ← i ₁ i ₀	Selects memory banks.		

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